Listing of Claims

The following listing of claims will replace all prior versions, and listings, of claims in the subject application:

1. (amended) A semiconductor storing device in which a row of memory cells is selected by a word line stage and a division word line stage, comprising:

memory arrays that each include a plurality of memory cells arranged in a matrix;

word lines for respective rows of the memory cells;

division word lines each of which is connected to the memory cells arranged in one row corresponding to one word;

division word line selectors that select the division word lines, respectively, the division word lines being connected to the respective word lines via the division word line selectors, respectively;

pairs of bit lines for reading data from the memory cells and writing data to the memory cells that are connected to the pairs of the bit lines, respectively;

column gates connected to the pairs of bit lines, respectively;

pairs of data lines that are connected to the pairs of bit lines via the column gates, respectively, to communicate data;

write buffers for data writing that are connected to the pairs of data lines, respectively;

sense operational amplifiers for data reading that are connected to the pairs of data

lines, respectively; and

data input/output circuits that are connected to the pairs of data lines via the write buffers and the sense operational amplifiers, respectively,

wherein input address data is specified by address data X[i:0], Y[j:0], and Z[k:0], two roots of selection signals for selecting the division word line selectors are provided alternately to the division word lines arranged in one of the memory arrays, and one of the two roots of the selection signals is enabled to select one of the division word line selectors in the one of the memory arrays, ~~and~~

~~eight roots of the selection signals in the entire semiconductor storing device are enabled so that when an address (z, y, x) is specified by the input address data X[i:0], Y[j:0], and Z[k:0], eight addresses of (z, y, x), (z, y, x+1), (z, y+1, x), (z, y+1, x+1), (z+1, y, x), (z+1, y, x+1), (z+1, y+1, x), and (z+1, y+1, x+1) are accessed simultaneously~~

the semiconductor storing device further comprises a decoder that receives the input address data X[i:0], Y[j:0], and Z[k:0], and causes two or four of the word lines provided in the respective rows of the memory cells to rise simultaneously, and

the semiconductor storing device has an address arrangement that enables eight addresses to be accessed simultaneously, the eight addresses being represented by (z, y, x), (z, y, x+1), (z, y+1, x), (z, y+1, x+1), (z+1, y, x), (z+1, y, x+1), (z+1, y+1, x), and (z+1, y+1, x+1) when (z, y, x) is specified by the input address data X[i:0], Y[j:0], and Z[k:0].

2. (original) The semiconductor storing device according to claim 1, further

comprising

selectors that are provided between the write buffers and the data input/output circuits, and between the sense operational amplifiers and the data input/output circuits, respectively such that the data input/output circuits always correspond one-to-one to the eight addresses of (z, y, x), (z, y, x+1), (z, y+1, x), (z, y+1, x+1), (z+1, y, x), (z+1, y, x+1), (z+1, y+1, x), and (z+1, y+1, x+1), respectively, and always transmit and receive, via the selectors, respective input data and output data corresponding one-to-one to the eight addresses, respectively.

3. (original) The semiconductor storing device according to claim 1, wherein when at least one of z, y, and x of the address (z, y, x) is an allowable maximum value, at least one of z+1, y+1, and x+1 that corresponds to the at least one of x, y, and z having the allowable maximum value is converted to "0" to access the eight addresses simultaneously.

4. (original) The semiconductor storing device according to claim 1, further comprising selection means for selecting either a first mode in which the eight addresses are accessed simultaneously, or a second mode in which a single address is accessed.

5. (amended) A semiconductor storing device in which a row of memory cells is selected by a word line stage and a division word line stage, comprising:

memory arrays that each include a plurality of memory cells arranged in a matrix;

word lines for respective rows of the memory cells;

division word lines each of which is connected to the memory cells arranged in one row corresponding to one word;

division word line selectors that select the division word lines, respectively, the division word lines being connected to the respective word lines via the division word line selectors, respectively;

pairs of bit lines for reading data from the memory cells and writing data to the memory cells that are connected to the pairs of the bit lines, respectively;

column gates connected to the pairs of bit lines, respectively;

pairs of data lines that are connected to the pairs of bit lines via the column gates, respectively, to communicate data;

write buffers for data writing that are connected to the pairs of data lines, respectively;

sense operational amplifiers for data reading that are connected to the pairs of data lines, respectively; and

data input/output circuits that are connected to the pairs of data lines via the write buffers and the sense operational amplifiers, respectively,

wherein input address data is specified by address data X[i:0], Y[j:0], and Z[k:0], four roots of selection signals for selecting the division word line selectors are provided to the division word lines arranged in one of the memory arrays, and one of the four roots of the selection signals is enabled to select one of the division word line selectors in the one of the

memory arrays, and

~~eight roots of the selection signals in the entire semiconductor storing device are enabled so that when an address (z, y, x) is specified by the input address data X[i:0], Y[j:0], and Z[k:0], eight addresses of (z, y, x), (z, y, x+1), (z, y+1, x), (z, y+1, x+1), (z+1, y, x), (z+1, y, x+1), (z+1, y+1, x), and (z+1, y+1, x+1) are accessed simultaneously~~

the semiconductor storing device further comprises a decoder that receives the input address data X[i:0], Y[j:0], and Z[k:0], and causes one, two or four of the word lines provided in the respective rows of the memory cells to rise simultaneously, and

the semiconductor storing device has an address arrangement that enables eight addresses to be accessed simultaneously, the eight addresses being represented by (z, y, x), (z, y, x+1), (z, y+1, x), (z, y+1, x+1), (z+1, y, x), (z+1, y, x+1), (z+1, y+1, x), and (z+1, y+1, x+1) when (z, y, x) is specified by the input address data X[i:0], Y[j:0], and Z[k:0].

6. (original) The semiconductor storing device according to claim 5, further comprising

selectors that are provided between the write buffers and the data input/output circuits, and between the sense operational amplifiers and the data input/output circuits, respectively such that the data input/output circuits always correspond one-to-one to the eight addresses of (z, y, x), (z, y, x+1), (z, y+1, x), (z, y+1, x+1), (z+1, y, x), (z+1, y, x+1), (z+1, y+1, x), and (z+1, y+1, x+1), respectively, and always transmit and receive, via the selectors, respective input data and output data corresponding one-to-one to the eight addresses,

respectively.

7. (original) The semiconductor storing device according to claim 5, wherein in a case where when the address (z, y, x) is specified, an address determined by at least one of z+1, y+1, and x+1 does not exist in the semiconductor storing device, the at least one of z+1, y+1, and x+1 is converted to "0" to access the eight addresses simultaneously

8. (original) The semiconductor storing device according to claim 5, further comprising selection means for selecting either a first mode in which the eight addresses are accessed simultaneously, or a second mode in which a single address is accessed.

Claims 9-12 (canceled).